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L5	218	(chapman near james). in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/31 15:57
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L7	162	buffer$1 and table$1 and ((last or end) near5 row$1) and 707/1,2,10,100.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/05/31 15:59

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1   A fast parallel reed-solomon decoder on a reconfigurable architecture

Arezou Koohi, Nader Bagherzadeh, Chengzi Pan
October 2003   CODES+ISSS '03: Proceedings of the 1st IEEE/ACM/IFIP international
conference on Hardware/software codesign and system synthesis
Publisher: ACM

Full text available: 📄 pdf(292.18 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 5,   Downloads (12 Months): 89,   Citation Count: 1

This paper presents a software implementation of a very fast parallel Reed-Solomon decoder on the second generation of MorphoSys reconfigurable computation platform, which is targeting on streamed applications such as multimedia and DSP. Numerous modifications ...

Keywords: Berlekamp algorithm, Chein search, Reed-Solomon codes, SIMD processor, reconfigurable architecture

2 Data memory minimization by sharing large size buffers

Hyunok Oh, Soonhoi Ha
January   ASP-DAC '00: Proceedings of the 2000 conference on Asia South Pacific
2000   design automation
Publisher: ACM

Full text available: pdf(76.93 KB)   Additional Information: full citation, references

Bibliometrics: Downloads (6 Weeks): 5,   Downloads (12 Months): 13,   Citation Count: 0

3 An Algorithmic Approach for Generic Parallel Adders

Jianhua Liu, Shuo Zhou, Haikun Zhu, Chung-Kuan Cheng
November   ICCAD '03: Proceedings of the 2003 IEEE/ACM international conference
2003   on Computer-aided design
Publisher: IEEE Computer Society

Full text available: pdf(244.18 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 10,   Downloads (12 Months): 64,   Citation Count: 4

Binary addition is the most fundamental and frequently used operation. A well-designed adder should be fast and satisfy the application requirements. We propose an algorithmic approach to generate an irregular parallel-prefix adder, which has minimal delay ...

4 A complexity effective communication model for behavioral modeling of signal processing applications

Satya Kiran, M. N. Jayram, Pradeep Rao, S. K. Nandy
June   DAC '03: Proceedings of the 40th conference on Design automation
2003
Publisher: ACM

Full text available: pdf(88.67 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1,   Downloads (12 Months): 24,   Citation Count: 2

In this paper, we argue that the address space of memory regions that participate in inter task communication is over-specified by the traditional communication models used in behavioral modeling, resulting in sub-optimal implementations. We propose ...

5 Energy-efficient signal processing using FPGAs

Seonil Choi, Ronald Scrofano, Viktor K. Prasanna, Ju-Wook Jang

February   FPGA '03: Proceedings of the 2003 ACM/SIGDA eleventh international
2003   symposium on Field programmable gate arrays

Publisher: ACM

Full text available: 📄 pdf(245.07   Additional Information: full citation, abstract, references, cited by,
                           KB)   index terms

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 94, Citation Count: 4

In this paper, we present techniques for energy-efficient design at the algorithm
level using FPGAs. We then use these techniques to create energy-efficient designs
for two signal processing kernel applications: fast Fourier transform (FFT) and
matrix ...

Keywords: FFT, FPGA, energy efficient design techniques, matrix multiplicaiton,
performance estimation

6 Texture compression using low-frequency signal modulation

Simon Fenney

July   HWWS '03: Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on
2003   Graphics hardware

Publisher: Eurographics Association

Full text available: 📄 pdf(1.51   Additional Information: full citation, abstract, references, cited by, index
                           MB)   terms

Bibliometrics: Downloads (6 Weeks): 11, Downloads (12 Months): 60, Citation Count: 7

This paper presents a new, lossy texture compression technique that is suited to
implementation on low-cost, low-bandwidth devices as well as more powerful
rendering systems. It uses a representation that is based on the blending of two (or
more) 'low ...

7 Built-in self-test for signal integrity

Mehrdad Nourani, Amir Attarha

June 2001 DAC '01: Proceedings of the 38th conference on Design automation

Publisher: ACM

Full text available: 📄 pdf(149.79   Additional Information: full citation, abstract, references, cited by,
                           KB)   index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 31, Citation Count: 3

Unacceptable loss of signal integrity may harm the functionality of SoCs permanently
or intermittently. We propose a systematic approach to model and test signal
integrity in deep-submicron high-speed interconnects. Various signal integrity
problems ...

8 Algorithmic foundations for a parallel vector access memory system

Binu K. Mathew, Sally A. McKee, John B. Carter, Al Davis
July   SPAA '00: Proceedings of the twelfth annual ACM symposium on Parallel
2000   algorithms and architectures
Publisher: ACM

Full text available: pdf(221.23 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 18, Citation Count: 1

This paper presents mathematical foundations for the design of a memory controller
subcomponent that helps to bridge the processor/memory performance gap for
applications with strided access patterns. The Parallel Vector Access (PVA) ...

9 Extending JTAG for Testing Signal Integrity in SoCs

N. Ahmed, M. Tehranipour, M. Nourani
March   DATE '03: Proceedings of the conference on Design, Automation and
2003   Test in Europe - Volume 1, Volume 1
Publisher: IEEE Computer Society

Full text available: pdf(143.66 KB)   Publisher   Additional Information: full citation, abstract,
Site   references, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 30, Citation Count: 0

As the technology is shrinking and the working frequency is going into multi
gigahertz range, the issues related to interconnect testing are becoming more
dominant. Specifically, signal integrity loss issues are becoming more important and
detection ...

10 Parallel execution for serial simulators

David Nicol, Philip Heidelberger
July   ACM Transactions on Modeling and Computer Simulation (TOMACS),
1996   Volume 6 Issue 3
Publisher: ACM

Full text available: pdf(450.56 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 38, Citation Count: 14

This article describes an approach to discrete event simulation modeling that appears
to be effective for developing portable and efficient parallel execution of models of
large distributed systems and communication networks. In this approach, the
modeler ...

Keywords: parallel simulation, simulation tools

11 Embedded cache architecture with programmable write buffer support for power and performance flexibility

Afzal Malik, Bill Moyer, Roger Zhou

October 2002   CASES '02: Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems

Publisher: ACM

Full text available: pdf(122.19 KB)   Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 30, Citation Count: 0

Next generation portable devices are placing stringent requirements on overall system power and performance. Voice recognition, streaming video and high speed wire¿less internet access are just some of the features being incorporated in these handheld ...

Keywords: cache control, cache management, copyback, programmable, push buffer, write buffer, writethrough

12 Signal integrity management in an SoC physical design flow

Murat Becer, Ravi Vaidyanathan, Chanhee Oh, Rajendran Panda

April 2003   ISPD '03: Proceedings of the 2003 international symposium on Physical design

Publisher: ACM

Full text available: pdf(163.22 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 37, Citation Count: 1

Signal integrity closure is one of the key challenges in DSM (Deep- SubMicron) physical design. In this paper, we propose a physical design methodology which includes signal integrity management through noise analysis and repair at multiple phases of ...

Keywords: crosstalk noise, noise avoidance, noise repair, signal integrity

13 Realization of a programmable parallel DSP for high performance image processing applications

Jens Peter Wittenburg, Willm Hinrichs, Johannes Kneip, Martin Ohmacht, Mladen Berekovi•, Hanno Lieske, Helge Kloos, Peter Pirsch

May 1998   DAC '98: Proceedings of the 35th annual conference on Design automation

Publisher: ACM

Full text available: pdf(2.35 MB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 50, Citation Count: 2

Architecture and design of the HiPAR-DSP, a SIMD controlled signalprocessor with parallel data paths, VLIW and novel memory design.The processor architecture is derived from an analysis of thetarget algorithms and specified in VHDL on register transfer ...

14 A checkpointing strategy for scalable recovery on distributed parallel systems

Vijay K. Naik, Samuel P. Midkiff, Jose E. Moreira
November   Supercomputing '97: Proceedings of the 1997 ACM/IEEE conference on
1997   Supercomputing (CDROM)
Publisher: ACM

Full text available: pdf(144.90 KB)   Additional Information: full citation, abstract, references

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 40, Citation Count: 0

In this paper, we describe a new scheme for checkpointing parallel applications on message-passing scalable distributed memory systems. The novelty of our scheme is that a checkpointed application can be restored, from its checkpointed state, in a reconfigured ...

Keywords: DRMS, IBM RS/6000 SP, checkpointing and restart, parallel checkpointing, reconfigurable checkpointing, scalable recovery

15 Interconnect design for deep submicron ICs

Jason Cong, Zhigang Pan, Lei He, Cheng-Kok Koh, Kei-Yong Khoo
November   ICCAD '97: Proceedings of the 1997 IEEE/ACM international conference
1997   on Computer-aided design
Publisher: IEEE Computer Society

Full text available: pdf(157.58 KB) Publisher   Additional Information: full citation, abstract,
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Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 42, Citation Count: 46

In this paper, we study the interconnect layout optimization problem under a higher-order RLC model to optimize not just delay, but also waveform for RLC circuits with non-monotone signal response. We propose a unified approach that considers topology ...

Keywords: required-arrival-time Steiner tree higher-order moment signal delay and integrity

16 Performance-impact limited area fill synthesis

Yu Chen, Puneet Gupta, Andrew B. Kahng
June 2003 DAC '03: Proceedings of the 40th conference on Design automation
Publisher: ACM

Full text available: 📄 pdf(98.23 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 21, Citation Count: 7

Chemical-mechanical planarization (CMP) and other manufacturing steps in very deep-submicron VLSI have varying effects on device and interconnect features, depending on the local layout density. To improve manufacturability and performance predictability, ...

Keywords: VLSI manufacturability, coupling capacitance extraction, dummy fill problem, greedy method, linear programming, signal delay

17 Parallelization and performance of 3D ultrasound imaging beamforming algorithms on modern clusters

F. Zhang, A. Bilas, A. Dhanantwari, K. N. Plataniotis, R. Abiprojo, S. Stergiopoulos
June   ICS '02: Proceedings of the 16th international conference on Supercomputing
2002
Publisher: ACM

Full text available: 📄 pdf(279.01 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 14, Downloads (12 Months): 116, Citation Count: 1

Recently there has been a lot of interest in improving the infrastructure used in medical applications. In particular, there is renewed interest on non-invasive, high-resolution diagnostic methods. One such method is digital, 3D ultrasound medical imaging. ...

Keywords: medical applications, parallel processing

18 Scalable flow control for multicast ABR services in ATM networks

Xi Zhang, Kang G. Shin, Debanjan Saha, Dilip D. Kandlur
February   IEEE/ACM Transactions on Networking (TON), Volume 10 Issue 1
2002
Publisher: IEEE Press

Full text available: 📄 pdf(706.72 KB)   Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 22, Citation Count: 2

We propose a flow-control scheme for multicast ABR services in ATM networks. At the heart of the proposed scheme is an optimal second-order rate control algorithm, called the α-*control,* designed to deal with the variation in RM-cell round-trip ...

Keywords: α-control, ABR, ATM, RTT variations, buffer control, feedback-soft synchronization (SSP), flow control, multicast, multicast flow control, scalability, second-order rate control, target buffer occupancy

19 Illuminating micro geometry based on precomputed visibility

Wolfgang Heidrich, Katja Daubert, Jan Kautz, Hans-Peter Seidel
July   SIGGRAPH '00: Proceedings of the 27th annual conference on Computer
2000   graphics and interactive techniques
Publisher: ACM Press/Addison-Wesley Publishing Co.

Full text available: 📄 pdf(4.35   Additional Information: full citation, abstract, references, cited by, index
MB)   terms

Bibliometrics: Downloads (6 Weeks): 3,   Downloads (12 Months): 37,   Citation Count: 17

Many researchers have been arguing that geometry, bump maps, and BRDFs present a hierarchy of detail that should be exploited for efficient rendering purposes. In practice however, this is often not possible due to inconsistencies in the illumination ...

Keywords: Monte Carlo techniques, frame buffer tricks, graphics hardware, illuminatiion effects, reflectance & shading models, texture mapping

20 Run-time adaptation in river

Remzi H. Arpaci-Dusseau
February   ACM Transactions on Computer Systems (TOCS),   Volume 21 Issue 1
2003
Publisher: ACM

Full text available: 📄 pdf(849.04
KB)   Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 6,   Downloads (12 Months): 61,   Citation Count: 2

We present the design, implementation, and evaluation of run-time adaptation within the River dataflow programming environment. The goal of the River system is to provide adaptive mechanisms that allow database query-processing applications to cope with ...

Keywords: Performance availability, clusters, parallel I/O, performance faults, robust performance, run-time adaptation

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